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Low Power Ring Oscillator Design in 130nm CMOS Technology

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Abstract: A temperature-stable, low-power ring oscillator design for implementation in an Application-Specific Integrated Circuit (ASIC) is presented. In this work, the design uses a new arrangement of chain delay elements consisting of a current-starved inverter and a CMOS capacitor. This power consumption improvement ring oscillator design was built in the environment of 130nm CMOS process technology using Mentor Graphics environment with voltage supply 1V. The simulation results show a maximum power consumption of 1.036 nW and it shows that the presented design is applicable in low power advanced sensing systems application including biomedical, chemical, and other sensors.

Keywords: *TCMOS, Ring Oscillator, Low Power*

INTRODUCTION

Wireless sensors and miniature electronics are important in monitoring the vital parameters of the human body and the Surrounding environment. These devices are particularly important to the elderly, children, pregnant women and the disabled. Wireless sensor systems can and do provide lifesaving assistance, particularly to these categories of patients. Advances in nanoelectronics and semiconductor technology have a rapid progress in the integration of nanosensors in ASIC (Application Specific Integrated Circuit) devices for biomedical, chemical, and other sensor applications [1] which implemented a fully integrated RF-powered contact lens with a single element display [2]. This led to the development of a smart lens technology capable of sensing glucose level from tear and informing the user [3].

Wireless sensors have also been widely used in personal health monitoring, environmental monitoring, structural health monitoring, and other applications [4]-[6]. Wireless sensors as such demand low-power readout systems with robust and reliable output that is independent of environmental conditions such as temperature. General purpose analog to digital converters (ADC) consume a relatively large amount of energy that limits the lifetime of low-power, wireless sensors. A ring oscillator-based read-out circuit presented in [7] translates change in a resistance into frequency (7 kHz/Ω) with a low power consumption of 1 mW.

A ring oscillator based read-out circuit reported in [8] uses a 180 nm CMOS technology with a relatively small chip area of 0.0077 mm2, and consumes 36μW power. Another ring oscillator-based CMOS temperature sensor reported by [9] is shown to have extremely low simulated power consumption of 3.476μW. The ring oscillator design presented in this paper addresses the need for further reduction in power consumption, for advanced miniature sensing systems.

METHODOLOGY

A conventional ring oscillator consists of an odd number of inverters (N) connected in series that form a closed loop path. The frequency of oscillation is determined by the overall delay in the inverter loop, which in turn is

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dependent on the delay in each inverter. The delay in an inverter is controlled by the current through the transistors that make up the inverter.

In the presented research, the current starved inverter with power switching, seen in conventional design, is replaced by current starved inverter with symmetrical load (Fig. 1 (a)). The symmetrical load generates higher current, increasing the sensitivity of the ring oscillator and providing higher frequency of oscillation. This may also make the inverter more sensitive to the temperature variation and power supply fluctuations, which are unfavorable characteristics for sensor chip applications. To improve the stability, a simple inverter is placed between two current starved inverters with symmetrical load as shown in Fig. 1(b).

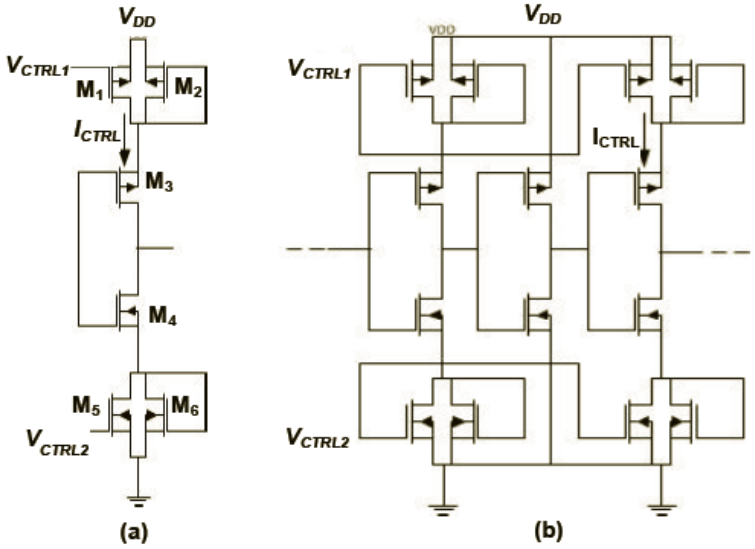

Fig 1 a) Current starved inverter with symmetrical load, b) Oscillator circuit.

Recent CMOS technology is in the range of several picoseconds for delay in an inverter. To dummy transistors are used as capacitors, which increase the delay at each stage by reducing the number of inverters in the oscillator. This will also to increase the system stability and dummy transistors are used as capacitors, which increase the delay at each stage. Dummy transistor (DM), shown in Fig. 2(a), provides delay control through the control voltage. As for figure 2(b), the dummy transistor is implemented after each current starved element. Thus, the ring oscillators presented in this paper consists of one delay dummy transistor units, and a current starved inverter with symmetrical load as shown in Fig. 2(c). A dummy transistor placed between the inverter and voltage-controlled delay elements also provides better temperature stability. The proposed CMOS ring oscillator was simulated with Mentor Graphic tool with 130 nm CMOS process parameters and 1V power supply. The ring oscillator includes 5 delays stages as shown in Fig. 2(c). Three of the delay units are voltage-controlled elements, where the first stage is controlled by input voltage (VCTRL) which in turn generates control voltage for the following two stages.

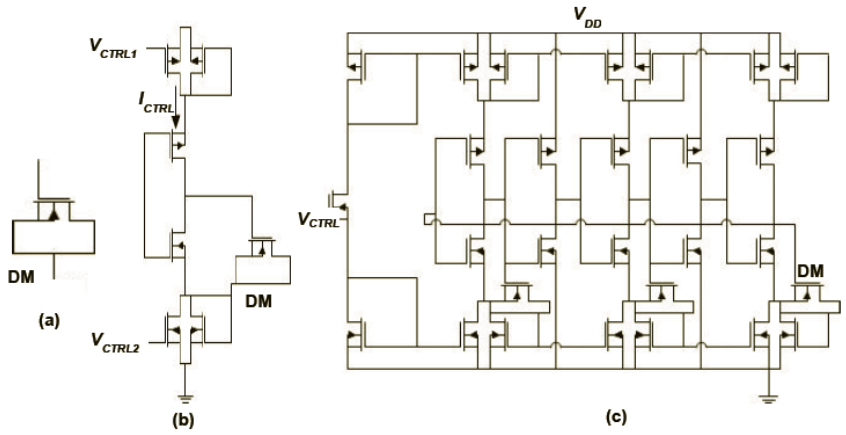

Fig 2 a) Dummy transistor, b) Delay stage with dummy transistor, c) The complete oscillator design

According to the downscaling CMOS process technique that has been used for this work, the gate length is reduced from the conventional of 180nm to 130nm. Reducing the gate length will overcome many drawbacks and provide better functions to the transistor itself. Shrinking of gate length will reduce the capacitance and the power supply voltage which is effective for lowering the power consumption.

Equation 1 & 2 shows the relationship of transistor sizing and the relationship of resistance with transistor sizing.

$$\mathbf{R} = \frac{\mathbf{Length,L}}{\mathbf{Width,W}} \mathbf{x} \frac{\mathbf{Resistivity,\rho}}{\mathbf{thickness,t}} = \frac{\mathbf{\rho/t}}{\mathbf{W/L}} = \frac{\mathbf{Sheet\ resistance,R_s}}{\mathbf{W/L}} \quad (\mathbf{1})$$

$$\boldsymbol{R\alpha \frac{1}{W/L}} \quad (\mathbf{2})$$

RESULT AND DISCUSSION

Proposed design has been verified in Mentor Graphics software to measure the output signal of proposed ring oscillator using ELDONET simulator. The input voltage Vin is set 5V and reference voltage Vref is 1V for simulating the outputs results. The circuit was sized according to the desired transistor sizing to improve the power consumption of the proposed design as shown in Figure 3.

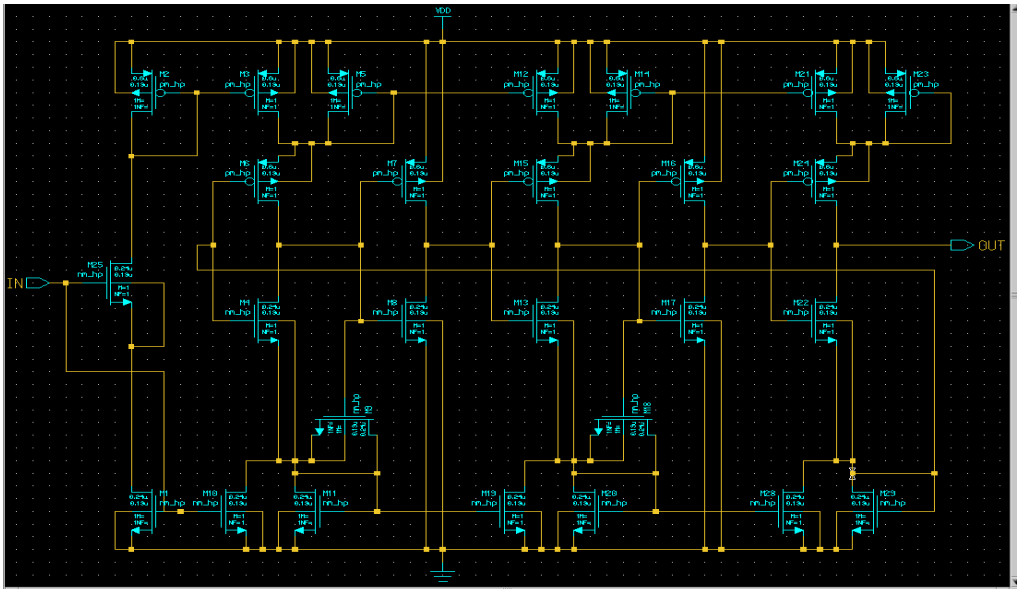

Fig 3 Schematic of the proposed design

Transistor Sizing

pMOS transistor has lower mobility than electron and must be sized larger to achieve comparable rising and falling delays The transistor sizing from [10] shows that it only used the ratio pMOS to nMOS width is 1:1. For our work, the width of the pMOS is doubled with the ratio of 2:1 to overcome the drawbacks of pMOS and to ensure that the PMOS will works almost the same speed as nMOS and hence, makes the resistance lower by referring to the equation in (2).

Simulated Waveform

Simulate waveform for proposed ring oscillator shown in Figure 4. The clock frequency proposed circuit design is 100MHz with 1V supply voltage (VDD) and input voltage. The output waveform smoother after modified transistor width using an optimization technique of transistor sizing.

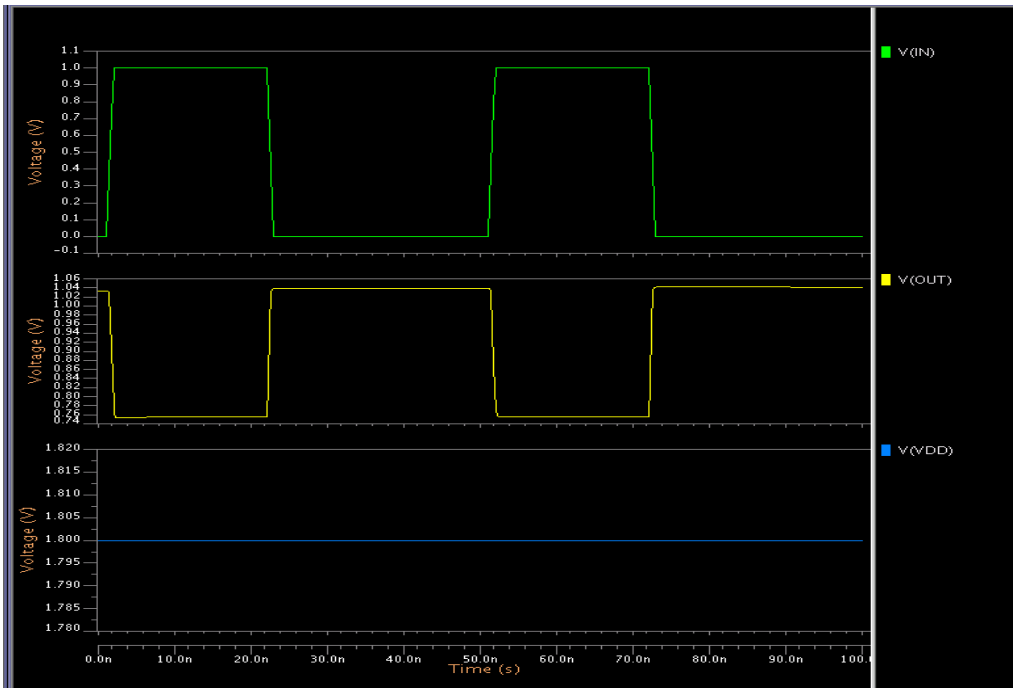

Fig 4 Simulation results of proposed comparator.

Power consumption

After simulates the proposed design as we set all the parameter at the test bench as in Figure 3 where the rise time and fall time are set to 1ps. This is to speed up the generations of the output pulses. For the power consumption, the proposed comparator consume about 1.036nW (Figure 5).

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   TOTAL POWER DISSIPATION:  1.0362N     WATTS


Eldo NEWTON: VNTOL=1.000000e-06 RELTOL=6.111111e-04

Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost UKMMentor20 -jwdbport 33314

Compute from 0.000000 Nano to 100.000000 Nano
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Fig 5 Power consumption of the proposed ring oscillator

Table 1 Summary of ring oscillator performance.

Item	Value
Technology	0.13μm
Supply Voltage	1V
Power Consumption	1.036nW
Sampling rate	100MHz

The performance comparisons of CMOS comparator in various technologies had been shown in Table 3. Compared to others research works, it is observed that the proposed comparator circuit has lower power consumption compare to the other two journal comparator as the number of transistor and the width of the transistor is different.

Table 2 Performance comparison of ring oscillator

Year Published [Ref. No.]	CMOS process (um)	Power
2012[8]	0.18	36 µW
2016[9]	0.18	3.476 µW
This work	0.13	1.036 nW

CONCLUSION

This paper was proposed the low power ring oscillator design, by using transistor sizing technique and gate length reduction. This design is implemented in Mentor Graphics environment using CMOS 130nm process technology with voltage supply 1V. The design has produced very low power consumption equal to 1.036 nW. This design maintains circuit stability and showed that it can be used for the application that required less power consuming.

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